IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Douglas R. Hackler, Sr. et al. Confirmation No. 8539

Application No. 10/733,612

Filed: December 11, 2003

For: **SRAM CELL**

Group Art Unit: 2818

Examiner:

Date: May 7, 2004

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

TO THE COMMISSIONER FOR PATENTS:

1. Pursuant to the duty of disclosure, documents listed on the accompanying Form PTO-1449 (or equivalent) are presented for the Examiner's consideration.

   ☒ Copies of listed documents are enclosed. (37 CFR § 1.98(a))

   ☐ Copies of listed U.S. patent documents are omitted because this application was filed after June 30, 2003 and is, thus, subject to image file wrapper processing. Copies of listed foreign patent documents and non-patent literature are enclosed.

   ☐ Copies of the documents listed on sheet(s) _____ of Form PTO-1449 (or equivalent) are omitted because (1) they are already of record in U.S. Patent Application No. _____, filed _____, on which this application relies for an earlier filing date under 35 U.S.C. § 120; and (2) any information disclosure statement filed in the prosecution of Application No. _____, complies with 37 CFR §§ 1.98(a) through (c). (37 C.F.R. § 1.98(d))

2. ☐ The Examiner's attention is directed to the enclosed copy of copending U.S. Patent Application No. _____, filed _____, for _____, which is cited in this application.

3. This information disclosure statement is being submitted (check box a., b., or c.):

   a. ☒ Within three months of the filing date of a national application or entry of the national stage in an international application; or before the mailing of a first Office action on the merits; or before the mailing of a first Office action after the filing of a request for continued examination under 37 CFR 1.114. (No statement under 37 CFR 1.97(e) is required.); or

b. ☐ After the period set forth in paragraph 3a, but before the mailing date of either a final action, a notice of allowance, or an action that otherwise closes prosecution in the application. (Check box i. or ii.)

i. ☐ A $180.00 information disclosure statement submission fee set forth in 37 CFR 1.17(p) is enclosed, or

ii. ☐ A statement specified by 37 CFR 1.97(e) is set forth below; or

c. ☐ After the mailing date of a final action or notice of allowance and on or before payment of the issue fee. A statement specified by 37 CFR 1.97(e) is set forth below. Enclosed is a $180.00 information disclosure statement processing fee set forth in 37 CFR 1.17(p).

4. If a statement specified by 37 CFR 1.97(e) is required, the attorney or agent signing below hereby states that:

☐ each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; or

☐ no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement.

5. ☐ A concise explanation of the relevance of each document not in the English language and/or selected documents in the English language is set forth below.

Respectfully submitted,

By _____
John R. Thompson
Registration No. 40,842

STOEL RIVES LLP
One Utah Center Suite 1100
201 S Main Street
Salt Lake City, UT 84111-4904
Telephone: (801) 328-3131
Facsimile: (801) 578-6999
Attorney Docket No. 51889/4

Sheet 1 of 2

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 51889/4 US	APPLICATION NO. 10/733,612
INFORMATION DISCLOSURE CITATION		APPLICANT – Douglas R. Hackler, Sr. et al.	
Title: **SRAM Cell**		FILING DATE- December 11, 2003	

OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication , etc.)

	1	van Meer et al., "70 nm Fully-Depleted SOI CMOS Using a New Fabrication Scheme: The Spacer/Replacer Scheme," 2002 IEEE, 2002 Symposium On VLSI Technology Digest of Technical Papers, pgs. 170-171.
	2	Baze et al., "A Digital CMOS Design Technique for SEU Hardening," IEEE Transactions on Nuclear Science, Vol. 47, No. 6, December 2000, pgs. 2603-2608.
	3	Khare et al., "A High Performance 90nm SOI Technology with 0.992 μm^2 6T-SRAM Cell," 2002 IEEE, pgs. 16.1.1-16.1.4.
	4	Ootsuka et al., "A Novel 0.20 μm Full CMOS SRAM Cell Using Stacked Cross Couple with Enhanced Soft Error Immunity," 1998 IEEE, pgs. 8.3.1-8.3.4.
	5	Cox et al., "A Partially Depleted 1.8V SOI CMOS SRAM Technology Featuring a 3.77 μm^2 Cell," 2000 IEEE, 2000 Symposium on VLSI Technology Digest of Technical Papers, pgs. 170-171.
	6	Ikeda et al., "A Soft Error Immune 0.35 μm PD-SOI SRAM Technology Compatible with Bulk CMOS," Proceedings 1998 IEEE International SOI Conference, October 1998, pgs. 159-160.
	7	Warren et al., "Analysis of the Influence of MOS Device Geometry on Predicted SEU Cross Sections," IEEE Transactions on Nuclear Science, Vol. 46, No. 6, December 1999, pgs. 1363-1369.
	8	Dodd et al., "Basic Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics," IEEE Transactions on Nuclear Science, Vol. 50, No. 3, June 2003, pgs. 583-602.
	9	Schwank et al., "BUSFET – A Radiation-Hardened SOI Transistor," IEEE Transactions on Nuclear Science, Vol. 46, No. 6, December 1999, pgs. 1809-1816.
	10	Shaneyfelt et al., "Challenges in Hardening Technologies Using Shallow-Trench Isolation," IEEE Transactions on Nuclear Science, Vol. 45, No. 6, December 1998, pgs. 2584-2592.
	11	Gasiot et al., "Comparison of the Sensitivity to Heavy Ions of 0.25-μm Bulk and SOI Technologies," IEEE Transactions on Nuclear Science, Vol. 49, No. 3, June 2002, pgs. 1450-1455.
	12	Sung et al., "Design of an Embedded Fully-Depleted SOI SRAM," 2001 IEEE, pgs. 13-18.
	13	Zhang et al., "Double-Gate Fully-Depleted SOI Transistors for Low-Power High-Performance Nano-Scale Circuit Design," pgs. 213-218.
	14	Brady et al., "Evaluation of the Performance and Reliability of a 1M SRAM on Fully-Depleted SOI," Proceedings 1998 IEEE International SOI Conference, October 1998, pgs. 129-130.
	15	Hirano et al., "High Soft-Error Tolerance Body-Tied SOI Technology with Partial Trench Isolation (PTI) for Next Generation Devices," 2002 IEEE, 2002 Symposium On VLSI Technology Digest of Technical Papers, pgs. 48-49.
	16	Hirano et al., "Impact of Actively Body-bias Controlled (ABC) SOI SRAM by using Direct Body Contact Technology for Low-Voltage Application," 2003 IEEE, pgs. 2.4.1-2.4.4.
	17	Hazucha et al., "Impact of CMOS Technology Scaling on the Atmospheric Neutron Soft Error Rate," IEEE Transactions on Nuclear Science, Vol. 47, No. 6, December 2000, pgs. 2586-2594.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformation with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	18	Leray et al., "Impact of Technology Scaling in SOI Back-Channel Total Dose Tolerance, a 2-D Numerical Study Using Self-Consistent Oxide Code," IEEE Transactions on Nuclear Science, Vol. 47, No. 3, June 2000, pgs. 620-626.
	19	Tosaka et al., "Measurement and Analysis of Neutron-Induced Soft Errors in Sub-Half-Micron CMOS Circuits," IEEE Transactions on Electron Devices, Vol. 45, No. 7, July 1998, pgs. 1453-1458.
	20	Sexton et al., "Precursor Ion Damage and Angular Dependence of Single Event Gate Rupture in Thin Oxides," IEEE Transactions on Nuclear Science, Vol. 45, No. 6, December 1998, pgs. 2509-2518.
	21	Liu et al., "Proton Induced Single Event Upset In A 4M SOI SRAM," 2003 IEEE, pgs. 26-27.
	22	Schwank et al., "Radiation Effects in SOI Technologies," IEEE Transactions on Nuclear Science, Vol. 50, No. 3, June 2003, pgs. 522-538.
	23	Hirose et al., "SEU Resistance in Advanced SOI-SRAMs Fabricated by Commercial Technology Using a Rad-Hard Circuit Design," IEEE Transactions on Nuclear Science, Vol. 49, No. 6, December 2002, pgs. 2965-2968.
	24	Dodd et al., "SEU-Sensitive Volumes in Bulk and SOI SRAMs From First-Principles Calculations and Experiments," IEEE Transactions on Nuclear Science, Vol. 48, No. 6, December 2001, pgs. 1893-1903.
	25	Gasiot et al., "SEU Sensitivity of Bulk and SOI Technologies to 14-MeV Neutrons," IEEE Transactions on Nuclear Science, Vol. 49, No. 6, December 2002, pgs. 3032-3037.
	26	Dodd et al., "Single-Event Upset and Snapback in Silicon-on-Insulator Devices and Integrated Circuits," IEEE Transactions on Nuclear Science, Vol. 47, No. 6, December 2000, pgs. 2165-2174.
	27	Cohen et al., "Soft Error Considerations for Deep-Submicron CMOS Circuit Applications," 1999 IEEE, pgs. 13.1.1-13.1.4.
	28	Milanowski et al., "TCAD-Assisted Analysis of Back-Channel Leakage in Irradiated Mesa SOI nMOSFETs," IEEE Transactions on Nuclear Science, Vol. 45, No. 6, December 1998, pgs. 2593-2599.
	29	Ferlet-Cavrois et al., "Total Dose Induced Latch in Short Channel NMOS/SOI Transistors," IEEE Transactions on Nuclear Science, Vol. 45, No. 6, December 1998, pgs. 2458-2466.
	30	Ferlet-Cavrois et al., "Worst-Case Bias During Total Dose Irradiation of SOI Transistors," IEEE Transactions on Nuclear Science, Vol. 47, No. 6, December 2000, pgs. 2183-2188.
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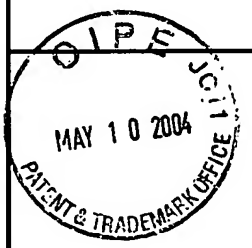
CERTIFICATE OF MAILING BY FIRST CLASS MAIL (37 CFR 1.8) Applicant(s): **Douglas R. Hackler, Sr. et al.**	Docket No. **51889/4**

Serial No.	Filing Date	Examiner	Group Art Unit
10/733,612	**December 11, 2003**		**2818**

Invention:

SRAM CELL



I hereby certify that this **Supplemental Information Disclosure Statement;(see below):**
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